ABSTRACT

A programmable logic device includes a routing structure, which takes the form of multiple distributed OR gates, which are positioned within the device to allow signals to be input from spaced apart logic elements, and present the input signals to other logic elements, which, again, may be spaced apart throughout the device. Each of the distributed OR gates, and its connections to the other logic elements, acts as a multiplexer. Sufficient of these distributed OR gates are provided to allow a bus structure to be implemented within the device. Since the OR gates are provided separately from the logic elements of the programmable logic device, the required bus structure can be implemented more efficiently.